TRANSMITTAL OF APPEAL BRIEF	Docket No. M4065.0210/P210

In re Application of: Sam Yang et al.

Application No.	Filing Date	Examiner	Group Art Unit
09/588,008-Conf. #9015	June 6, 2000	H. B. Trinh	2814

Invention: A CAPACITOR FOR A SEMICONDUCTOR DEVICE

TO THE COMMISSIONER OF PATENTS:

Transmitted herewith is the Appeal Brief in this application, with respect to the Notice of Appeal filed: March 22, 2007 .

The fee for filing this Appeal Brief is $ 500.00 .

[X] Large Entity [ ] Small Entity

[ ] A petition for extension of time is also enclosed.

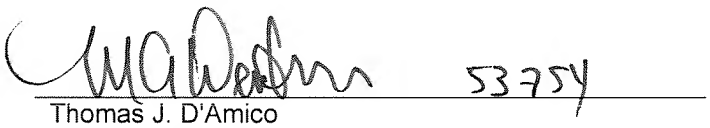
The fee for the extension of time is _____ .

[ ] A check in the amount of _____ is enclosed.

[ ] Charge the amount of the fee to Deposit Account No. 04-1073 .
This sheet is submitted in duplicate.

[ ] Payment by credit card. Form PTO-2038 is attached.

[X] The Director is hereby authorized to charge any additional fees that may be required or credit any overpayment to Deposit Account No. 04-1073 .
This sheet is submitted in duplicate.



53754

Dated: June 25, 2007

Thomas J. D'Amico
Attorney Reg. No. : 28,371
DICKSTEIN SHAPIRO LLP
1825 Eye Street, NW
Washington, DC 20006-5403
(202) 420-2232

Docket No.: M4065.0210/P210
(PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:
Sam Yang et al.

Application No.: 09/588,008 Confirmation No.: 9015

Filed: June 6, 2000 Art Unit: 2814

For: A CAPACITOR FOR A SEMICONDUCTOR DEVICE Examiner: H. B. Trinh

APPEAL BRIEF

MS Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

As required under § 41.37(a), this brief is filed in furtherance of the Notice of Appeal.

The fees required under § 41.20(b)(2) are dealt with in the accompanying TRANSMITTAL OF APPEAL BRIEF.

This brief contains items under the following headings as required by 37 C.F.R. § 41.37 and M.P.E.P. § 1205.2:

Appendix B Evidence (None beyond cited references)
Appendix C Related Proceedings

I. REAL PARTY IN INTEREST

The real party in interest for this appeal is:

MICRON TECHNOLOGY, INC.

II. RELATED APPEALS AND INTERFERENCES

There is related appeal in case in U.S. Pat. Appl. No. 10/281,954, a divisional application of the present application, which could affect or be directly affected by or have a bearing on the Board's decision in this appeal. There is also related case U.S. Pat. Appl. No. 10/002,176, which is another divisional application of the present application and currently stands rejected under a non-final Office Action.

There are no other appeals, interferences, or judicial proceedings known to the undersigned which will directly affect or be directly affected by or have a bearing on the Board's decision in this appeal.

III. STATUS OF CLAIMS

A. Total Number of Claims in Application

There are 32 claims pending in application.

B. Current Status of Claims

1. Claims canceled: 32-98

2. Claims withdrawn from consideration but not canceled: None.

3. Claims pending: 1-31 and 99

4. Claims allowed: --[1]

5. Claims rejected: 1-31 and 99[2]

C. Claims On Appeal

The claims on appeal are claims 1-31 and 99.

IV. STATUS OF AMENDMENTS

Applicant filed an Amendment After Final Rejection on December 19, 2006. The Examiner responded to the Amendment After Final Rejection in an Advisory Action mailed January 12, 2007. In the Advisory Action, the Examiner indicated that Applicants' proposed amendments to the claims would be entered for the purposes of the Appeal. However, Applicants did not propose any amendments to the claims in the paper filed December 19, 2006.

Accordingly, the claims enclosed herein as Appendix A reflect the current status of the claims prior to the December 19, 2006 paper.

V. SUMMARY OF CLAIMED SUBJECT MATTER

Independent claims 1 and 99 are pending. The subject matter defined by claims 1 and 99 is described in the specification at least on page 6, line 6 to page 8, line 22 and in FIG. 1 (the relevant portion of FIG. 1 produced below). Independent claims 1 and 99 are directed to a

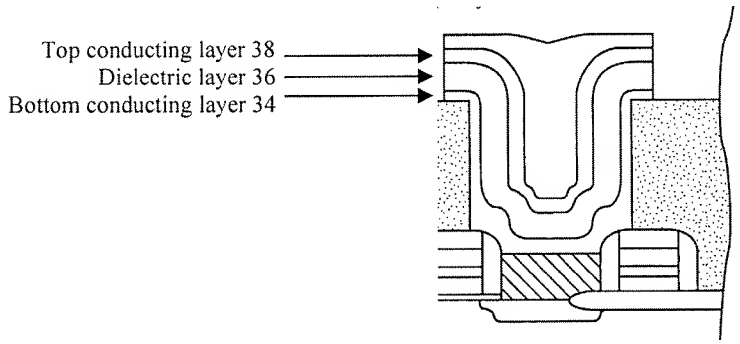
---

[1] The Papers from the PTO are inconsistent and therefore it is unclear if any of the claims are allowable. According to the most recently issued Advisory Action in this case, mailed March 21, 2007, part of Paper No. 20070317, claims 1-31 and 99 stand rejected. In the Notice of Panel Decision from Pre-Appeal Brief Review, mailed March 24, 2007, part of Paper No. 20070522, claims 1-3, 7-16, 18-25, 29-31, and 99 stand rejected. The Notice does not indicate the status of claims 4-6, 17, and 26-28. For the purposes of the Appeal and out of an abundance of caution, Applicants presume claims 1-31 and 99 stand rejected. However, Applicants are not suggesting that claims 4-6, 17, and 26-28 are not in condition of allowance.

[2] See Footnote #1.

capacitor. Referring to Fig. 1 of the application, reproduced in part below, a stacked capacitor is built over a substrate. The capacitor has a bottom conducting layer 34, a dielectric layer 36, and a top conducting layer 38. See, specification at page 7, line 4 to page 8, line 12. After the bottom conducting layer 34 and the dielectric layer 36 are deposited but before the top conducting layer 38 is deposited, a first anneal is performed. After the top conducting layer 38 is deposited, a second anneal is performed. See, specification at page 7, line 4 to page 8, line 12.

The claimed invention is directed towards reducing current leakage and increasing the dielectric constant. In conventional methods, the formation of the dielectric layer contains defects such as oxygen vacancies. The claimed invention attempts to solve these problems by performing two anneals to overcome defects that occur during formation of the dielectric and formation of the upper electrode. Thus one anneal is performed after the formation of the dielectric and another after formation of the upper electrode.



Claim 1 recites, *inter alia*, a capacitor for a semiconductor device, said capacitor comprising: "a bottom conducting layer, wherein said bottom conducting layer is a bottom electrode; an annealed dielectric layer formed over said bottom conducting layer, wherein said annealed dielectric layer is annealed with a first annealing process; and a top electrode consisting of a single oxidized gas annealed top conducting layer formed over said annealed dielectric layer, wherein said annealed top conducting layer is annealed with a second annealing process."

Support for the "bottom conducting layer, wherein said bottom conducting layer is a bottom electrode..." can be found at least in the specification at page 6, line 6 to page 7, line 7 and FIG. 1, referring to bottom electrode 34.

Support for the "an annealed dielectric layer formed over said bottom conducting layer, wherein said annealed dielectric layer is annealed with a first annealing process..." can be found at least in the specification at page 6, line 6 to page 8, line 2 and FIG. 1, referring to dielectric layer 36.

Support for the "top electrode consisting of a single oxidized gas annealed top conducting layer formed over said annealed dielectric layer, wherein said annealed top conducting layer is annealed with a second annealing process" can be found at least in the specification at page 6, line 6 to page 8, line 10 and FIG. 1, referring to top conducting layer 38.

Claim 99 recites, *inter alia*, a capacitor for a semiconductor device, said capacitor comprising: "a bottom electrode; an annealed dielectric layer formed over said bottom electrode that has been annealed with a first oxidizing gas anneal process; and an upper electrode comprising a top conducting layer which is an oxidized gas annealed layer formed over said annealed dielectric layer that has been annealed with a second oxidizing gas anneal process."

Support for the "a bottom electrode" can be found at least in the specification at page 6, line 6 to page 7, line 7 and FIG. 1, referring to bottom electrode 34.

Support for the "an annealed dielectric layer formed over said bottom electrode that has been annealed with a first oxidizing gas anneal process" can be found at least in the specification at page 6, line 6 to page 8, line 2 and FIG. 1, referring to dielectric layer 36.

Support for the "an upper electrode comprising a top conducting layer which is an oxidized gas annealed layer formed over said annealed dielectric layer that has been annealed with a second oxidizing gas anneal process" can be found at least in the specification at page 6, line 6 to page 8, line 10 and FIG. 1, referring to upper electrode 38.

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

Claims 1-3, 7-16, 18-25, 29-31 and 99 stand rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,338,996 ("Iizuka").

Claims 4, 5 and 17 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Iizuka in view of U.S. Patent No. 5,452,178 ("Emesh").

Claims 6 and 14 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Iizuka in view of U.S. Patent No. 6,303,426 ("Alers").

Claims 26 and 27 stand rejected under 35 U.S.C. § 102(e) as anticipated by Iizuka, or in the alternative, under 35 U.S.C. § 103(a) as obvious over Iizuka, in view of U.S. Patent No. 6,475,854 ("Narwankar").

Claim 28 stands rejected under 35 U.S.C. § 102(e) as anticipated by or Iizuka, in the alternative, under 35 U.S.C. § 103(a) as obvious over Iizuka, in view of U.S. Patent No. 6,387,802 ("Marsh").

VII. ARGUMENT

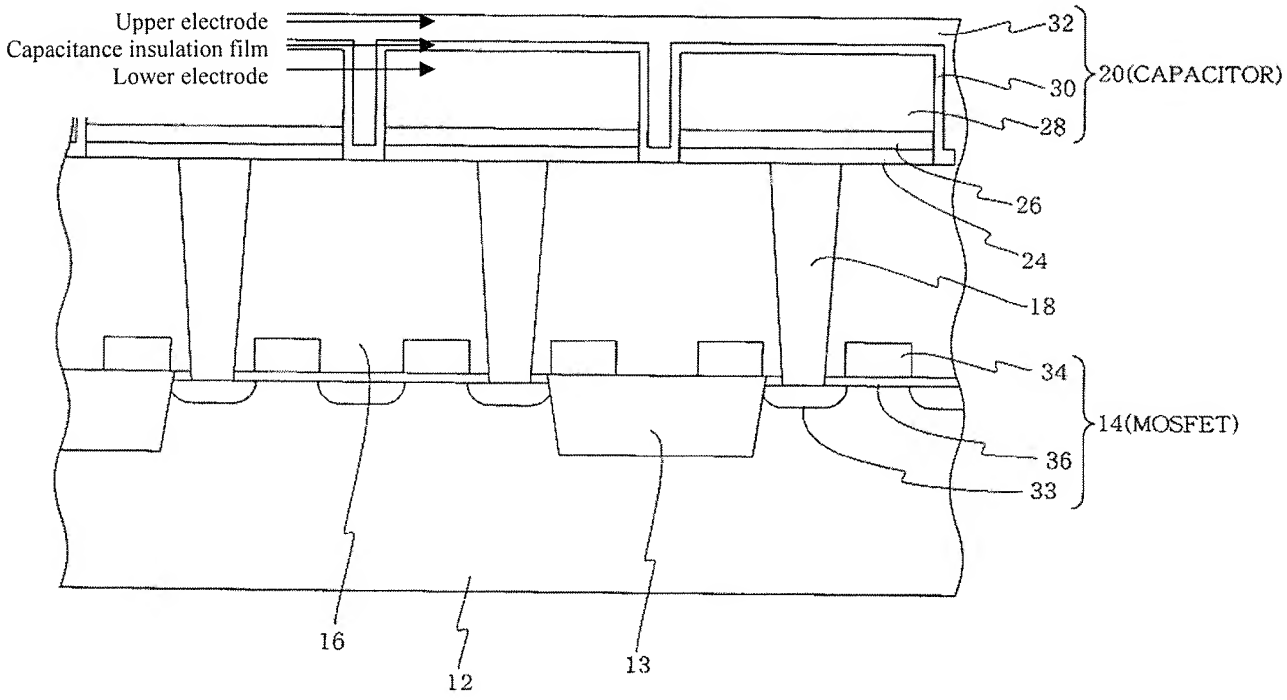
Claims 1-3, 7-16, 18-25, 29-31 and 99 are not anticipated by U.S. Patent No. 6,338,996 ("Iizuka").

Claim 1 recites a capacitor comprising, *inter alia*, "a bottom conducting layer . . . an *annealed dielectric layer*, wherein said annealed dielectric layer is annealed with a *first annealing process* . . . and a top electrode consisting of a single oxidized *gas annealed top conducting layer* formed over said *annealed* dielectric layer, wherein said annealed top conducting layer is annealed with *a second annealing process*," (emphasis added).

Iizuka discloses a method of producing a semiconductor memory device having a capacitor formed of a high dielectric insulation film and a noble metal upper electrode which are

successively layered on a noble metal lower electrode and after the upper electrode is formed, the capacitor is annealed (Iizuka, Summary of the invention)

FIG. 1



As depicted Iizuka's Fig. 1, a capacitor 20 according to Iizuka is formed from a lower electrode 28, dielectric insulation layer 30, and an upper electrode 32. (Iizuka, col. 3, p. 35- 40)

Iizuka does not disclose all the limitations of claim 1. Specifically, Iizuka does *not* disclose an *annealed* dielectric layer "annealed with a first annealing process" *and* an annealed top electrode "annealed with a second annealing process".

The Office suggests in the Action mailed September 22, 2006 that the first annealing process is disclosed by Iizuka at col. 1, lines, 30-35, col. 2, lines 13-15; col. 4, lines 55-60. The

Office also suggests in the Action mailed September 22, 2006 that the second annealing process is disclosed by Iizuka at col. 2, line 33; and col. 5, lines 20-25. (cited passages set out below)

With respect to the claimed invention's "annealed dielectric layer", the Office offers:

Iizuka at col. 1, lines 30-35 ("Passage1"), which recites:

> After this, in order to get rid of peeling of the lower electrode, the BST thin film is crystallized with the RTA processing at 700 degrees C. in nitrogen. Next, a noble metal upper electrode using Ru or the like is formed to obtain a thin film capacitor. Then, with a known procedure, surface treatment is performed including formation of a passivation film.

and Iizuka at col. 2, lines 13-15 ("Passage2"), which recites:

> [Moreover, in order to lower the anneal temperature, Japanese Patent Publication 10-189908 discloses an invention in which the crystallized BST is formed by sputter of 550 degrees C. and a metal oxide film is formed before] post-anneal is performed in an oxygen atmosphere of 2 to 10 atmospheric pressure, for example, at a temperature of 500 degrees C. [However, even if the anneal is performed at 500 degrees C., there arise the problems of peel-off and conductivity defects.]

and Iizuka at col. 4, lines 55-60 ("Passage3"), which recites:

> In the second embodiment, after the high dielectric thin film capacitor is formed, anneal is performed in a gas mixture of oxygen (5% or below) and nitrogen at temperature of 300 to 400 degrees C. for about 40 minutes.

Passage1 is part of the background section of the Iizuka patent application as part of a general discussion of allegedly known annealing techniques. Passage1 refers generally refers to annealing a BST thin film, then forming the top electrode. There is no disclosure of a second anneal process for the upper electrode. Similarly, Passage2 is also part of the background section of Iizuka and also refers to forming and then annealing a BST layer. Once again, there is no disclosure of a second anneal process for the upper electrode. Passage3 refers to a second embodiment of Iizuka where an anneal process is performed after the capacitor structure is formed. Significantly, each of

these three passages refer to a single annealing process that occurs during or after the formation of the capacitor structure. Moreover, only Passage3 relates to an actual description of the Iizuka process.

With respect to the claimed invention's "second annealing process", the Office proffers:

Iizuka at col. 2, line 33 ("Passage4") which recites:

> [The present invention provides a semiconductor memory device production method for a semiconductor memory device having a capacitor formed by a high dielectric insulation film and a noble metal upper electrode which are successively layered on a noble metal lower electrode, the method being characterized in that the formation of the] capacitor is followed by anneal in a nitrogen atmosphere of 1 atmospheric pressure at temperature of 300 to 400 degrees [C.] [emphasis added]

and Iizuka at col. 5, line 20-25("Passage5"), which recites:

> Moreover, as has been described above, in the second embodiment, after the upper electrode is formed, anneal is performed in a mixture atmosphere of oxygen concentration of 0 to 5% and nitrogen.

Passage4 refers to a first embodiment of Iizuka where an anneal is performed after the capacitor is formed. No description is provided for providing an annealed dielectric layer which is annealed by a first anneal process before the anneal of the formed capacitor.

Passage5 is similar to Passage3, *supra*, and refers to the second embodiment of Iizuka where, once again, an anneal is performed after the capacitor is formed, but with anneal processing parameters different from those used for the anneal in the first embodiment. Thus, the difference between Iizuka's first embodiment and the second embodiment are in the annealing parameters: In the first embodiment, annealing is performed in a nitrogen atmosphere of 1 atmospheric pressure at temperature of 300 to 400 degrees C. In the second embodiment, annealing is performed in a gas mixture atmosphere of oxygen concentration of 5% or below and nitrogen under 1 atmospheric pressure at temperature of 300 to 400 degrees C. Significantly, Passage4 and Passage5 refer to a single annealing process which occurs after formation of the capacitor structure. The Office has not

shown, because it can not, an annealed dielectric "annealed with a first annealed process" and a top electrode annealed with a second annealing process.

As noted, the claimed invention is directed towards reducing current leakage and increasing the dielectric constant by performing two anneals to overcome defects that occur during formation of the dielectric and after formation of the upper electrode. Thus a first anneal is performed after the formation of the dielectric and a second anneal is performed after formation of the upper electrode.

Iizuka is directed towards solving the problem of leak currents, which may be reduced by performing an anneal of a capacitor "so as to assure a sufficient crystallization of the dielectric film and a stable leak current characteristic." (Iizuka, Col. 1, lines 54-56). However, high temperature anneals cause additional problems, including increased defects and peeling off under the contact portion of the lower electrode. (Iizuka, Col. 1, lines 59-64). Iizuka attempts to solve the problems by performing a low temperature anneal. Thus, Iizuka is attempting to solve a different problem than that addressed by the claimed invention.

Hence, at best, Iizuka only discloses one anneal performed, at a temperature lower than conventionally done, after the capacitor is formed. (See Iizuka specification for further description of only one anneal being performed in the method of Iizuka, that being after the capacitor structure is formed: "...the formation of the capacitor is followed by anneal..." (Iizuka, Abstract); "...the method being characterized in that the formation of the capacitor is followed by anneal..." (Iizuka, Col. 2, lines 30-32); "...the method being characterized in that the formation of the capacitor is followed by anneal..." (Iizuka, Col. 2, lines 41-43); "After forming the high dielectric thin film capacitor, anneal is performed..." (Iizuka, Col. 4, lines 28-30); "...after the high dielectric thin film capacitor is formed, anneal is performed..." (Iizuka, Col. 4, lines 57-59); and "As has been described above, according to the present invention, after formation of the capacitor, anneal is performed..." (Iizuka, Col. 5, lines 49-52).)

Additionally, during an Office interview held on February 21, 2007 in related case 10/002,176, the Office could not expressly identify the two annealing processes as claimed. Subsequent responses from the Office have not further identified in Iizuka a capacitor formed with two annealing processes.

Since the Office cannot identify in Iizuka "an *annealed dielectric layer*, wherein said annealed dielectric layer is annealed with a *first annealing process* . . ." and a "top electrode consisting of a single oxidized *gas annealed top conducting layer* formed over said *annealed* dielectric layer, wherein said annealed top conducting layer is annealed with *a second annealing process*," Iizuka cannot anticipate claim 1. In the Office Action dated September 22, 2006, the Office suggested that the "anneal" limitations of claim 1 are product-by-process limitations which are accorded little or no weight. However, claim 1 recites annealed structures in which the annealed structures have been annealed by two distinct anneal processes.

Since Iizuka does not disclose all the limitations of claim 1, claim 1 and claims 2-3, 7-16, 18-25 and 29-31 depending therefrom are not anticipated by Iizuka.

Claim 99 recites similar limitations to claim 1, including, *inter alia*, "an annealed dielectric layer . . . that has been annealed with a first oxidizing gas anneal process; and an upper electrode . . . which is an oxidized gas annealed layer formed over said annealed dielectric layer that has been annealed with a second oxidizing gas anneal process." For at least the same reasons as discussed with respect to claim 1, claim 99 is not anticipated by Iizuka.

A reversal of the rejections of claims 1-3, 7-16, 18-25, 29-31, and 99 as being anticipated by Iizuka is respectfully requested.

Claims 4, 5 and 17 are not unpatentable under 35 U.S.C. § 103(a) over Iizuka in view of U.S. Patent No. 5,452,178 ("Emesh").

Claim 4 recites, *inter alia*, "...wherein said bottom conducting layer is formed of a metal alloy."

Claim 5 recites, *inter alia*, "...wherein said bottom conducting layer is formed of a conducting metal oxide."

Claim 17 recites, *inter alia*, "...wherein said top conducting layer is formed of a conducting metal oxide."

Claims 4, 5 and 17 depend from claim 1 and are similarly allowable with claim 1 for at least the reasons provided above with regard to claim 1.

As discussed above, Iizuka does not teach or suggest a capacitor comprising, *inter alia*, "a bottom conducting layer . . . an *annealed dielectric layer*, wherein said annealed dielectric layer is annealed with a *first annealing process* . . . and a top electrode consisting of a single oxidized *gas annealed top conducting layer* formed over said *annealed* dielectric layer, wherein said annealed top conducting layer is annealed with *a second annealing process*," as recited in claim 1 (emphasis added).

Emesh discloses forming a capacitor within a via hole. Emesh does not cure the deficiency of Iizuka as Emesh does not teach or suggest the subject matter of claim 1.

Furthermore, the Office Action asserts that "it would have been obvious to one of ordinary skill in the art . . . to modify the bottom electrode of Iizuka with the metal alloy or conductive metal oxide material, as taught by Emesh, so as to provide an alternative material to make the bottom electrode." However, Iizuka *teaches away* from this combination. Iizuka discloses a "semiconductor device having a capacitor formed by a high dielectric insulation film and a *noble metal* upper electrode which are successively layered on a *noble metal* lower electrode." Col. 2, lines 28-31; Col. 2, lines 38-40. (Emphasis added). Iizuka specifically discloses that "[t]he lower electrode 28 *and* the upper electrode 28 are formed by a *noble metal film* such as Ru, Ir, and Pt." Col. 3, lines 38-40. (Emphasis added). Iizuka does not disclose the claim 4 limitation that the bottom conducting layer being formed from "a metal alloy," the claim 5 limitation that the bottom conducting layer being formed from "a conducting metal oxide," and the claim 17 limitation that the top conducting layer being formed from "a conducting metal oxide."

Since Iizuka teaches that *both* electrodes in the capacitor should consist of a *noble metal*, Iizuka teaches away from substituting Emesh's metal alloy, or a conducting metal oxide for either the upper or lower electrodes, and thus there is no motivation to combine the teachings of Iizuka and Emesh.

Since the cited references do not teach or suggest all the limitations of claim 1, claims 4, 5 and 17 depending therefrom are patentable over the reference. Furthermore, the Office has not identified any motivation in either Emesh or Iizuka to combine their divergent teachings in order to achieve the claimed invention or ignore the express teachings in Iizuka of using noble metal electrode for both the top and bottom electrodes of a capacitor.

Accordingly, a reversal of the § 103 rejection of claims 4, 5, and 17 is respectfully requested.

Claims 6 and 14 are not unpatentable under 35 U.S.C. § 103(a) over Iizuka in view of U.S. Patent No. 6,303,426 ("Alers").

Claim 6 recites, *inter alia*, "...wherein said bottom conducting layer is formed of a metal nitride."

Claim 14 recites, *inter alia*, "....wherein said top conducting layer is formed of a material selected from the noble metal group."

Claims 6 and 14 depend from claim 1 and should be similarly allowable with claim 1 for at least the reasons provided above with regard to claim 1, and on their own merits. As discussed above, Iizuka does not teach or suggest a capacitor comprising, *inter alia*, "a bottom conducting layer . . . an *annealed dielectric layer*, wherein said annealed dielectric layer is annealed with a *first annealing process* . . . and a top electrode consisting of a single oxidized *gas annealed top conducting layer* formed over said *annealed* dielectric layer, wherein said annealed top conducting layer is annealed with *a second annealing process*," as recited in claim 1 (emphasis added).

Alers discloses "a method of forming a capacitor in a semiconductor wafer having a plurality of stacked layers including a substrate, a first dielectric layer including a via that extends through the first dielectric layer and contacts the substrate." (Alers, Summary of the invention)

Alers does not cure the deficiency of Iizuka as Alers does not disclose a capacitor formed by two separate anneal processes.

The Office Action asserts that "it would have been obvious to one of ordinary skill in the art . . . to modify the invention of Iizuka with the bottom electrode made of metal nitride, as taught by Alers, so as to provide an alternative material for the bottom electrode." However, as noted above, Iizuka *teaches away* from such a combination, requiring use of noble metals for upper and lower electrodes. As such, Alers cannot be combined with Iizuka since Iizuka teaches away from any material other than noble metals for a bottom electrode. Accordingly, the references do not teach or suggest all the limitations of claim 1 and claims 6 and 14 depending therefrom.

Accordingly, a reversal of the § 103 rejection of claims 6 and 14 is respectfully requested.

Claims 26 and 27 are not anticipated under 35 U.S.C. § 102(e) by Iizuka, or in the alternative, unpatentable under 35 U.S.C. § 103(a) as obvious over Iizuka, in view of U.S. Patent No. 6,475,854 ("Narwankar").

Claim 26 recites, *inter alia*, "...wherein said annealed top conducting layer is a plasma enhanced annealed top conducting layer."

Claim 27 recites, *inter alia*, "...wherein said annealed top conducting layer is a remote plasma enhanced annealed top conducting layer."

Claims 26 and 27 depend indirectly from claim 1 and should be similarly allowable with claim 1 for at least the reasons provided above with regard to claim 1, and on their own merits. As discussed above, Iizuka does not teach or suggest a capacitor comprising, *inter alia*, "a bottom

conducting layer . . . an *annealed dielectric layer*, wherein said annealed dielectric layer is annealed with a *first annealing process* . . . and a top electrode consisting of a single oxidized *gas annealed top conducting layer* formed over said *annealed* dielectric layer, wherein said annealed top conducting layer is annealed with *a second annealing process*," as recited in claim 1 (emphasis added).

Accordingly, to the extent that this rejection is one of anticipation by Iizuka, a reversal is respectfully requested.

Narwankar discloses "A capacitor structure comprising a bottom electrode, an insulator and a top electrode, and method for manufacturing the same. The bottom and top electrodes preferably include a metal portion and a conducting oxygen-containing metal portion. In one embodiment, a layer of ruthenium is deposited to form a portion of the bottom electrode. Prior to deposition of the insulator, the ruthenium is annealed in an oxygen-containing environment. The insulator is then deposited on the oxygen-containing ruthenium layer. Formation of the top electrode includes depositing a first metal on the insulator, annealing the first metal and then depositing a second metal. The first and second metals may be ruthenium." (Narkwankar, Abstract)

Narwankar discloses a plasma enhanced annealed layer, but does not disclose "an *annealed dielectric layer*, wherein said annealed dielectric layer is annealed with a *first annealing process* . . . and a top electrode consisting of a single oxidized *gas annealed top conducting layer* formed over said *annealed* dielectric layer, wherein said annealed top conducting layer is annealed with *a second annealing process*," as recited in claim 1. Since neither Iizuka nor Narwankar, teach or suggest all the limitations of claim 1, claims 26 and 27 depending therefrom are patentable over the references. Accordingly, to the extent that this rejection is under § 103 based on the teachings of Iizuka in view of Narwankar, a reversal is respectfully requested.

Claim 28 is not anticipated under 35 U.S.C. § 102(e) by Iizuka or, in the alternative, unpatentable under 35 U.S.C. § 103(a) as obvious over Iizuka, in view of U.S. Patent No. 6,387,802 ("Marsh").

Claim 28 recites, *inter alia*, "...wherein said annealed top conducting layer is an ultraviolet light enhanced annealed top conducting layer."

Claim 28 depends from claim 1 and is similarly allowable with claim 1 for at least the reasons provided above with regard to claim 1, and on its own merits. As discussed above, Iizuka does not teach or suggest a capacitor comprising, *inter alia*, "a bottom conducting layer . . . an *annealed dielectric layer*, wherein said annealed dielectric layer is annealed with a *first annealing process* . . . and a top electrode consisting of a single oxidized *gas annealed top conducting layer* formed over said *annealed* dielectric layer, wherein said annealed top conducting layer is annealed with *a second annealing process*," as recited in claim 1 (emphasis added).

Iizuka also fails to disclose an ultraviolet enhanced annealed top electrode and this can not anticipated claims 28 for this additional revision. Accordingly, to the extent that the rejection of claim 28 is based on anticipation by Iizuka, a reversal of the rejection is respectfully requested.

Marsh discloses "A method of depositing a platinum based metal film by CVD deposition includes bubbling a non-reactive gas through an organic platinum based metal precursor to facilitate transport of precursor vapor to the chamber. The platinum based film is deposited onto a non-silicon bearing substrate in a CVD deposition chamber in the presence of ultraviolet light at a predetermined temperature and under a predetermined pressure. The film is then annealed in an oxygen atmosphere at a sufficiently low temperature to avoid oxidation of substrate. The resulting film is free of silicide and consistently smooth and has good step coverage." (Marsh, Abstract)

Marsh also fails to cure the inadequacies of Iizuka and fails to disclose Iizuka does not teach or suggest a capacitor comprising, *inter alia*, "a bottom conducting layer . . . an *annealed dielectric layer*, wherein said annealed dielectric layer is annealed with a *first annealing process* . . . and a top electrode consisting of a single oxidized *gas annealed top conducting layer* formed over said *annealed* dielectric layer, wherein said annealed top conducting layer is annealed with *a second annealing process*," as recited in claim 1 (emphasis added). Nor has there been provided in the references, the motivation or ability to combine the references to achieve the claimed invention.

Accordingly, to the extent that the rejection of claim 28 is under § 103 based on the teachings of Iizuka in view of Marsh, a reversal of the rejection is respectfully requested.

For the reasons advanced, claims 1-31 and 99 are not anticipated by or rendered obvious over the prior art cited in the various rejections of the claims. Accordingly, a reversal of all rejections is respectfully requested.

VIII. CLAIMS

A copy of the claims involved in the present appeal is attached hereto as Appendix A.

Dated: June 25, 2007

Respectfully submitted,

By _____

Thomas J. D'Amico
Registration No.: 28,371
Michael A. Weinstein
Registration No.: 53,754
DICKSTEIN SHAPIRO LLP
1825 Eye Street, NW
Washington, DC 20006-5403
(202) 420-2200
Attorney for Applicant

APPENDIX A

Claims Involved in the Appeal of Application Serial No. 09/588,008

1. A capacitor for a semiconductor device, said capacitor comprising:

a bottom conducting layer, wherein said bottom conducting layer is a bottom electrode;

an annealed dielectric layer formed over said bottom conducting layer, wherein said annealed dielectric layer is annealed with a first annealing process; and

a top electrode consisting of a single oxidized gas annealed top conducting layer formed over said annealed dielectric layer, wherein said annealed top conducting layer is annealed with a second annealing process.

2. The capacitor of claim 1, wherein said bottom conducting layer is formed of a material selected from the noble metal group.

3. The capacitor of claim 1, wherein said bottom conducting layer is formed of a metal.

4. The capacitor of claim 1, wherein said bottom conducting layer is formed of a metal alloy.

5. The capacitor of claim 1, wherein said bottom conducting layer is formed of a conducting metal oxide.

6. The capacitor of claim 1, wherein said bottom conducting layer is formed of a metal nitride.

7. The capacitor of claim 1, wherein said bottom conducting layer is formed of a material selected from the group consisting of: Platinum (Pt), Platinum Rhodium (PtRh), Platinum Iridium (PtIr), Ruthenium, Ruthenium Oxide (RuO_2), Rhodium Oxide (RhO_2). Chromium Oxide

(CrO_2), Molybdenum Oxide (MoO_2), Rhemium Oxide (ReO_3), Iridium Oxide (IrO_2), Titanium Oxides (TiO_1 or TiO_2), Vanadium Oxides (VO_1 or VO_2), Niobium Oxides (NbO_1 or NbO_2), and Tungsten Nitride (WNx, WN, or W2N).

8. The capacitor of claim 7, wherein said bottom conducting layer is formed of a material selected from the group consisting of: Platinum (Pt), Platinum Rhodium (PtRh), Platinum Iridium (PtIr), and Tungsten Nitride (WNx, WN, or W_2N).

9. The capacitor of claim 1, wherein said bottom conducting layer is placed on top of an oxygen barrier.

10. The capacitor of claim 1, wherein said dielectric layer is a dielectric metal oxide layer.

11. The capacitor of claim 1, wherein said dielectric layer has a dielectric constant between 7 and 300.

12. The capacitor of claim 1, wherein said dielectric layer is formed of a material selected from the group consisting of: Tantalum Oxide, Tantalum Pentoxide (Ta_2O_5), Barium Strontium Titanate (BST), Aluminum Oxide (Al_2O_3), Zirconium Oxide (ZrO_2), Praseodymium Oxide (PrO_2), Tungsten Oxide (WO_3), Niobium Pentoxide (Nb_2O_5), Strontium Bismuth Tantalate (BST), Hafnium Oxide (HfO_2), Hafnium Silicate, Lanthanum Oxide (La_2O_3), Yttrium Oxide (Y_2O_3) and Zirconium Silicate.

13. The capacitor of claim 12, wherein said dielectric layer is formed of a material selected from the group consisting of: Tantalum Oxide, Tantalum Pentoxide (Ta_2O_5), Barium Strontium Titanate (BST), Strontium Bismuth Tantalate (SBT), Aluminum Oxide (Al_2O_3), Zirconium Oxide (ZrO_2) and Hafnium Oxide (HfO_2).

14. The capacitor of claim 13, wherein said dielectric layer is Tantalum Oxide and is amorphous or crystalline.

15. The capacitor of claim 1, wherein said top conducting layer is formed of a material selected from the noble metal group.

16. The capacitor of claim 1, wherein said top conducting layer is formed of a non-oxidizing metal permeable to oxygen.

17. The capacitor of claim 1, wherein said top conducting layer is formed of a conducting metal oxide.

18. The capacitor of claim 1, wherein said top conducting layer is formed of a material selected from die group consisting of: Platinum (Pt), Platinum Rhodium (PtRh), Platinum Iridium (PtIr), Ruthenium, Ruthenium Oxide (RuO_2), Rhodium Oxide (RhO_2), Chromium Oxide (CrO_2), Molybdenum Oxide (MoO_2), Rhemium Oxide (ReO_3), Iridium Oxide (IrO2), Titanium Oxides (TiO_1 or TiO_2), Vanadium Oxides (VO_1 or VO_2), and Niobium Oxides (NbO_1 or NbO_2).

19. The capacitor of claim 18, wherein said top conducting layer is formed of a material selected from the group consisting of: Platinum (Pt), Platinum Rhodium (PtRh), and Platinum Iridium (PtIr).

20. The capacitor of claim 1, wherein said bottom and top conducting layers are formed of a material selected from the group consisting of: Platinum, Platinum Rhodium (PtRh), or Platinum Iridium (PtIr) and said dielectric layer is a layer of Tantalum Oxide.

21. The capacitor of claim 1, wherein said bottom and top conducting layers are formed of a material selected from the group consisting of Platinum, Platinum Rhodium (PtRh), or Platinum Iridium (PtIr) and, said dielectric layer is a layer of Barium Strontium Titanate (BST).

22. The capacitor of claim 1, wherein said top conducting layer is formed of a material selected from the group consisting of Platinum, Platinum Rhodium (PtRh), or Platinum Iridium (PtIr) and, said bottom conducting layer is a layer of Tungsten Nitride (WNx, WN, or W_2N) layer and, said dielectric layer is a layer of Aluminum Oxide (Al_2O_3).

23. The capacitor of claim 1, wherein said top conducting layer is annealed with an oxygen compound.

24. The capacitor of claim 23, wherein said oxygen annealed layer is one annealed in the presence of a material selected from the group consisting of: Oxygen (O_2), Ozone (O_3), Nitrous Oxide (N_2O), Nitric Oxide (NO), and water vapor (H_2O).

25. The capacitor of claim 23, wherein said oxygen annealed layer is one annealed in the presence of a gas mixture containing at least one element selected from the group consisting: Oxygen (O_2), Ozone (O_3), Nitrous Oxide (N_2O), Nitric Oxide (NO), and water vapor (H_2O).

26. The capacitor of claim 23, wherein said annealed top conducting layer is a plasma enhanced annealed top conducting layer.

27. The capacitor of claim 23, wherein said annealed top conducting layer is a remote plasma enhanced annealed top conducting layer.

28. The capacitor of claim 23, wherein said annealed top conducting layer is an ultraviolet light enhanced annealed top conducting layer.

29. The capacitor of claim 1, wherein said capacitor is a stacked capacitor.

30. The capacitor of claim 1, wherein further comprising an access transistor connected to said capacitor.

31. The capacitor of claim 1, wherein said capacitor forms part of a dynamic random access memory cell.

99. A capacitor for a semiconductor device, said capacitor comprising:

a bottom electrode;

an annealed dielectric layer formed over said bottom electrode that has been annealed with a first oxidizing gas anneal process; and

an upper electrode comprising a top conducting layer which is an oxidized gas annealed layer formed over said annealed dielectric layer that has been annealed with a second oxidizing gas anneal process.

APPENDIX B

(No Evidence beyond the cited references)

APPENDIX C

There is related appeal in case in divisional application U.S. Pat. Application. No. 10/281,954 which could affect or be directly affected by or have a bearing on the Board's decision in this appeal. The Appellate Brief in that case is being filed contemporaneously with this Brief. Related case U.S. Pat. Appl. No. 10/002,176, is another divisional application of the present application and currently stands rejected under a non-final Office Action.